



TJA1081

FlexRay node transceiver

Rev. 4 — 24 February 2011

Product data sheet

1. General description

The TJA1081 is a FlexRay node transceiver that is fully compliant with the FlexRay electrical physical layer specification V2.1 Rev. A (see [Ref. 1](#)). In addition, it incorporates features and parameters included in V3.0.1 (see [Ref. 2](#) and [Section 14](#)). It is primarily intended for communication systems from 1 Mbit/s to 10 Mbit/s, and provides an advanced interface between the protocol controller and the physical bus in a FlexRay network.

The TJA1081 features enhanced low-power modes, optimized for ECUs that are permanently connected to the battery.

The TJA1081 provides differential transmit capability to the network and differential receive capability to the FlexRay controller. It offers excellent EMC performance as well as high ESD protection.

The TJA1081 actively monitors system performance using dedicated error and status information (that can be read by any microcontroller), along with internal voltage and temperature monitoring.

The TJA1081 supports mode control as used in the TJA1080A (see [Ref. 3](#)).

2. Features and benefits

2.1 Optimized for time triggered communication systems

- Compliant with FlexRay electrical physical layer specification V2.1 Rev. A (see [Ref. 1](#))
- Automotive product qualification in accordance with AEC-Q100
- Data transfer up to 10 Mbit/s
- Support of 60 ns minimum bit time
- Very low ElectroMagnetic Emission (EME) to support unshielded cable
- Differential receiver with wide common-mode range for high ElectroMagnetic Immunity (EMI)
- Auto I/O level adaptation to host controller supply voltage V_{IO}
- Can be used in 14 V and 42 V powered systems
- Instant shut-down interface (via BGE pin)
- Independent power supply ramp-up for V_{BAT} , V_{CC} and V_{IO}

2.2 Low power management

- Low power management including inhibit switch
- Very low current in Sleep and Standby modes



- Local and remote wake-up
- Supports remote wake-up via dedicated data frames
- Wake-up source recognition

2.3 Diagnosis (detection and signalling)

- Overtemperature detection
- Short-circuit on bus lines
- V_{BAT} power-on flag (first battery connection and cold start)
- Pin TXEN and pin BGE clamping
- Undervoltage detection on pins V_{BAT} , V_{CC} and V_{IO}
- Wake source indication

2.4 Protection

- Bus pins protected against ± 8 kV HBM ESD pulses
- Bus pins protected against transients in automotive environment (according to ISO 7637 class C)
- Bus pins short-circuit proof to battery voltage (14 V and 42 V) and ground
- Fail-silent behavior in the event of an undervoltage on pins V_{BAT} , V_{CC} or V_{IO}
- Passive behavior of bus lines while the transceiver is not powered

2.5 Functional classes according to FlexRay electrical physical layer specification (see [Ref. 1](#))

- Bus driver voltage regulator control
- Bus driver - bus guardian control interface
- Bus driver logic level adaptation

3. Ordering information

Table 1. Ordering information

| Type number | Package | | Version |
|-------------|---------|---|----------|
| | Name | Description | |
| TJA1081TS | SSOP16 | SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm | SOT338-1 |

4. Block diagram

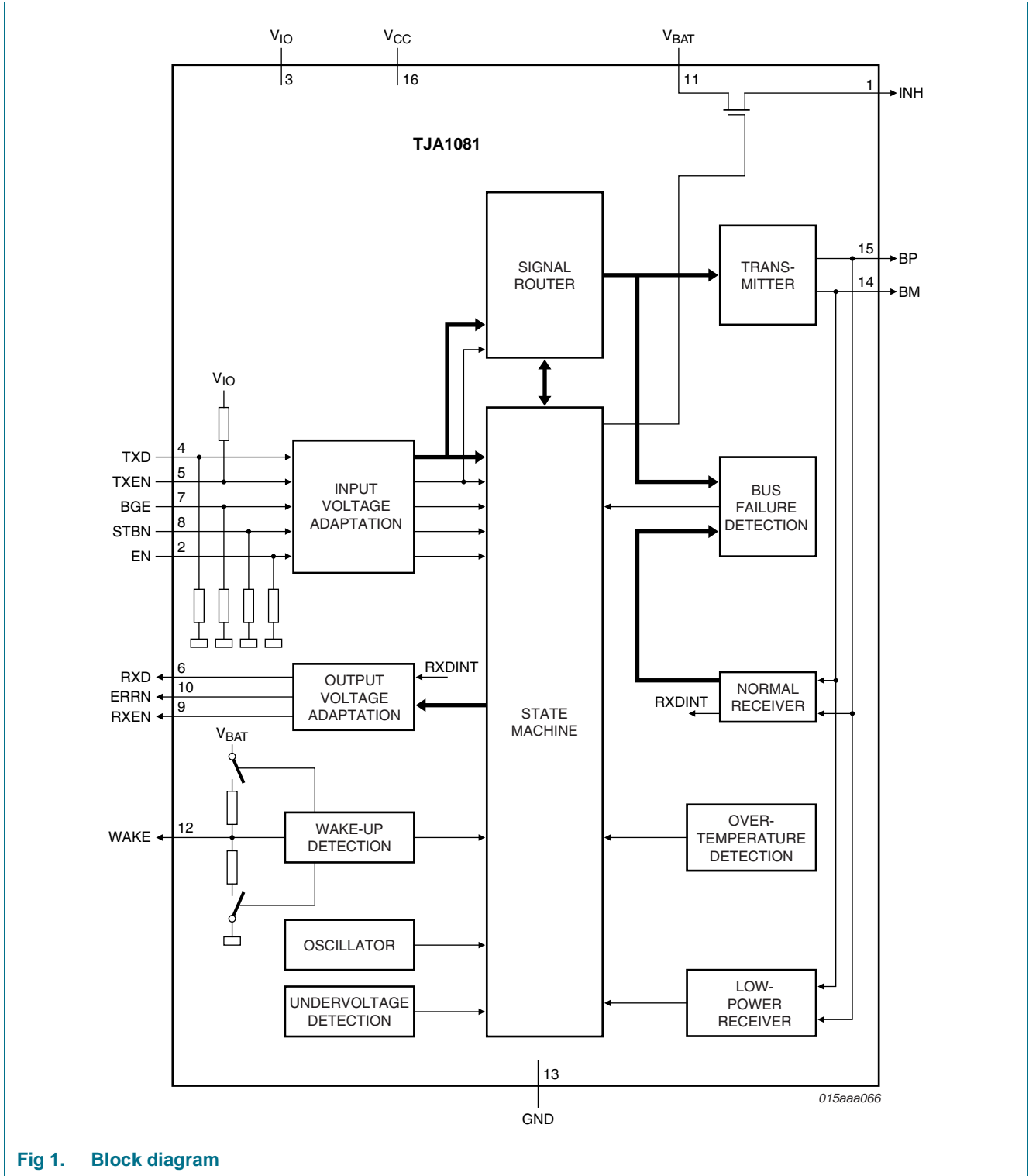


Fig 1. Block diagram

5. Pinning information

5.1 Pinning

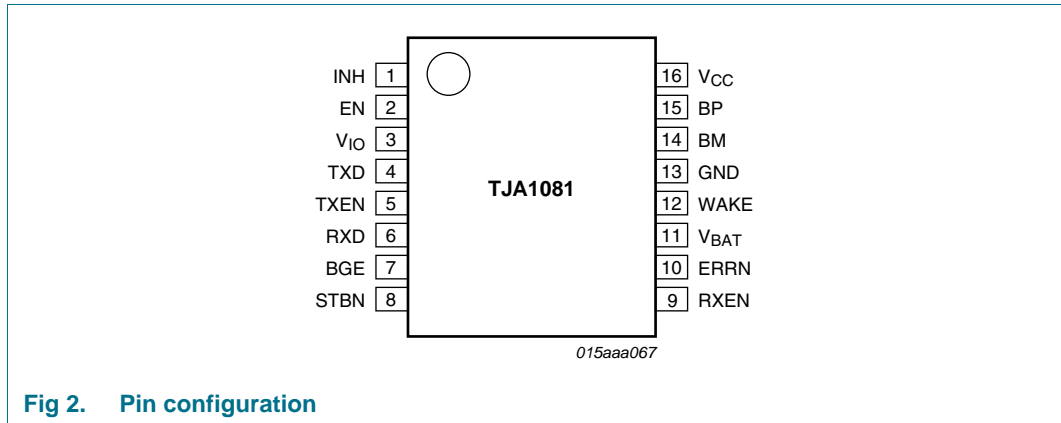


Fig 2. Pin configuration

5.2 Pin description

Table 2. Pin description

| Symbol | Pin | Type | Description |
|------------------|-----|------|---|
| INH | 1 | O | inhibit output for switching external voltage regulator |
| EN | 2 | I | enable input; enabled when HIGH; internal pull-down |
| V _{IO} | 3 | P | supply voltage for V _{IO} voltage level adaptation |
| TXD | 4 | I | transmit data input; internal pull-down |
| TXEN | 5 | I | transmitter enable input; when HIGH transmitter disabled; internal pull-up |
| RXD | 6 | O | receive data output |
| BGE | 7 | I | bus guardian enable input; when LOW transmitter disabled; internal pull-down |
| STBN | 8 | I | standby input; low-power mode when LOW; internal pull-down |
| RXEN | 9 | O | receive data enable output; when LOW bus activity detected |
| ERRN | 10 | O | error diagnoses output; when LOW error detected |
| V _{BAT} | 11 | P | battery supply voltage |
| WAKE | 12 | I | local wake-up input; internal pull-up or pull-down (depends on voltage at pin WAKE) |
| GND | 13 | P | ground |
| BM | 14 | I/O | bus line minus |
| BP | 15 | I/O | bus line plus |
| V _{CC} | 16 | P | supply voltage (+5 V) |

6. Functional description

The block diagram of the transceiver is shown in [Figure 1](#).

6.1 Operating modes

The TJA1081 supports the following operating modes:

- Normal (normal-power mode)
- Receive-only (normal-power mode)
- Standby (low-power mode)
- Go-to-sleep (low-power mode)
- Sleep (low-power mode)

6.1.1 Bus activity and idle detection

The following mechanisms for activity and idle detection are valid in normal-power modes:

- If the absolute differential voltage on the bus lines is higher than $|V_{i(dif)det(act)}|$ for $t_{det(act)(bus)}$, activity is detected on the bus lines and pin RXEN is switched LOW which results in pin RXD being released:
 - If, after bus activity detection, the differential voltage on the bus lines is higher than $V_{IH(dif)}$, pin RXD will go HIGH
 - If, after bus activity detection, the differential voltage on the bus lines is lower than $V_{IL(dif)}$, pin RXD will go LOW
- If the absolute differential voltage on the bus lines is lower than $|V_{i(dif)det(act)}|$ for $t_{det(idle)(bus)}$, then idle is detected on the bus lines and pin RXEN is switched to HIGH. This results in pin RXD being blocked (pin RXD is switched to HIGH or stays HIGH)

6.2 Mode control pins: STBN and EN

Control inputs STBN and EN are used to select the operating mode. See [Table 3](#) for a detailed description of pin signalling and [Figure 3](#) for the timing diagram.

All mode transitions are controlled via the STBN and EN pins, unless an undervoltage condition is detected. If V_{IO} and (V_{CC} or V_{BAT}) are within their specified operating ranges, pin ERRN will indicate the status of the error flag.

Table 3. Pin signalling

| Mode | STBN | EN | ERRN ^[1] | | RXEN | | RXD | | Transmitter | INH |
|--------------|------|------|-------------------------------|------------------|------------------------------|-----------------|------------------------------|--------------------|-------------|-------|
| | | | LOW | HIGH | LOW | HIGH | LOW | HIGH | | |
| Normal | HIGH | HIGH | error flag set | error flag reset | bus activity | bus idle | bus DATA_0 | bus DATA_1 or idle | enabled | HIGH |
| Receive-only | HIGH | LOW | | | | | | | disabled | |
| Go-to-sleep | LOW | HIGH | error flag set ^[2] | error flag reset | wake flag set ^[2] | wake flag reset | wake flag set ^[2] | wake flag reset | | |
| Standby | LOW | LOW | | | | | | | | |
| Sleep | LOW | X | | | | | | | | float |

[1] Pin ERRN provides a serial interface for retrieving diagnostic information.

[2] Valid if V_{IO} and (V_{CC} or V_{BAT}) are present.

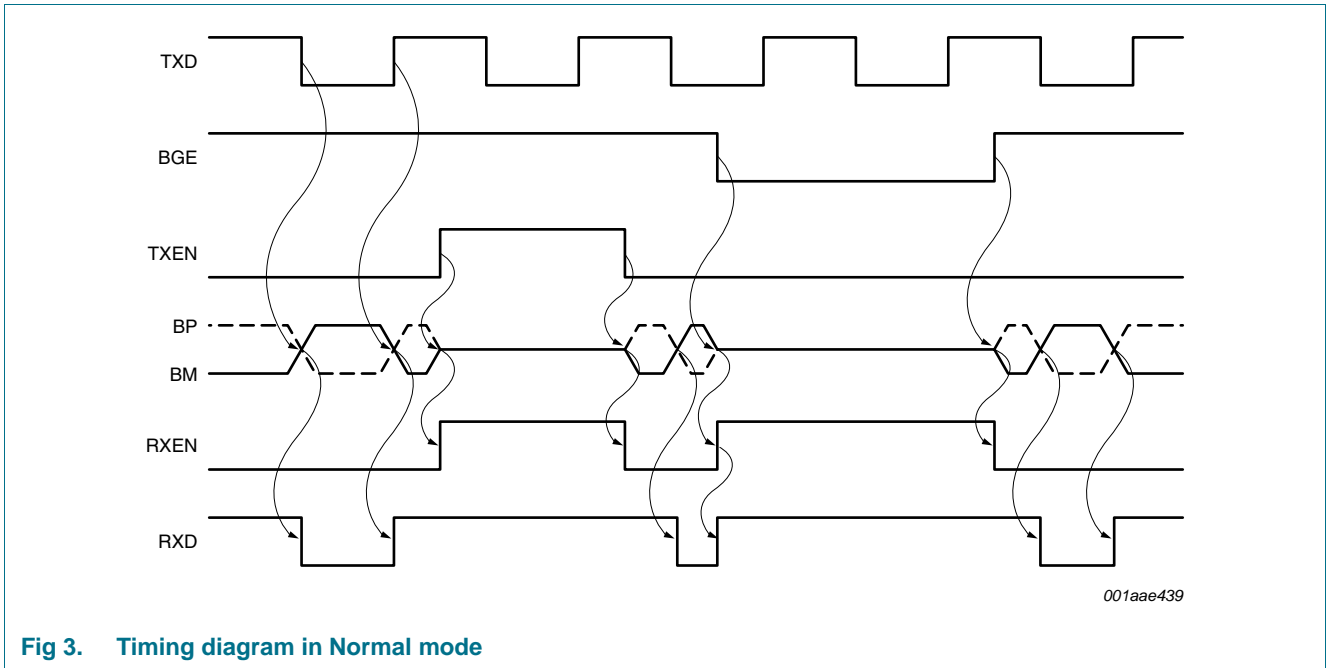


Fig 3. Timing diagram in Normal mode

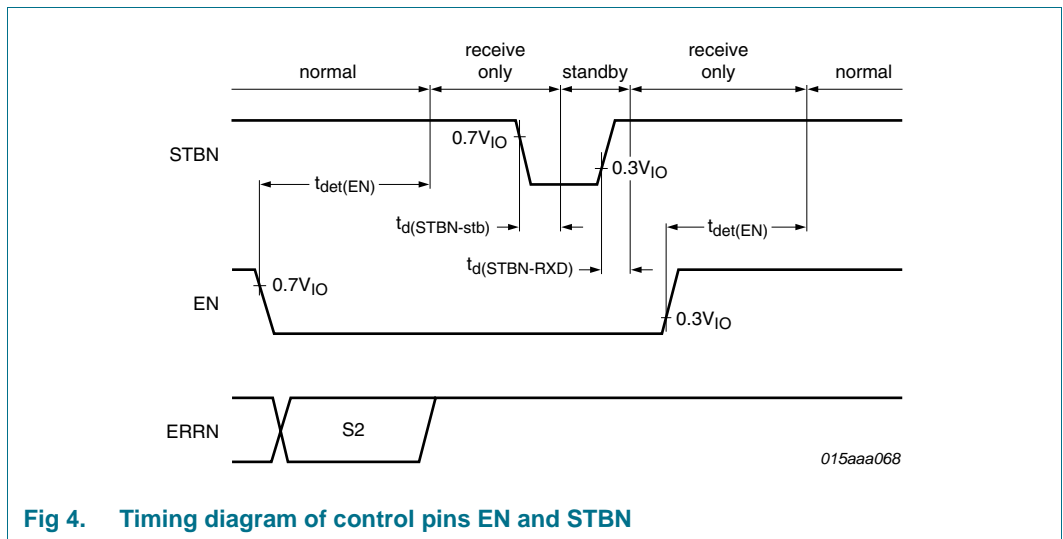
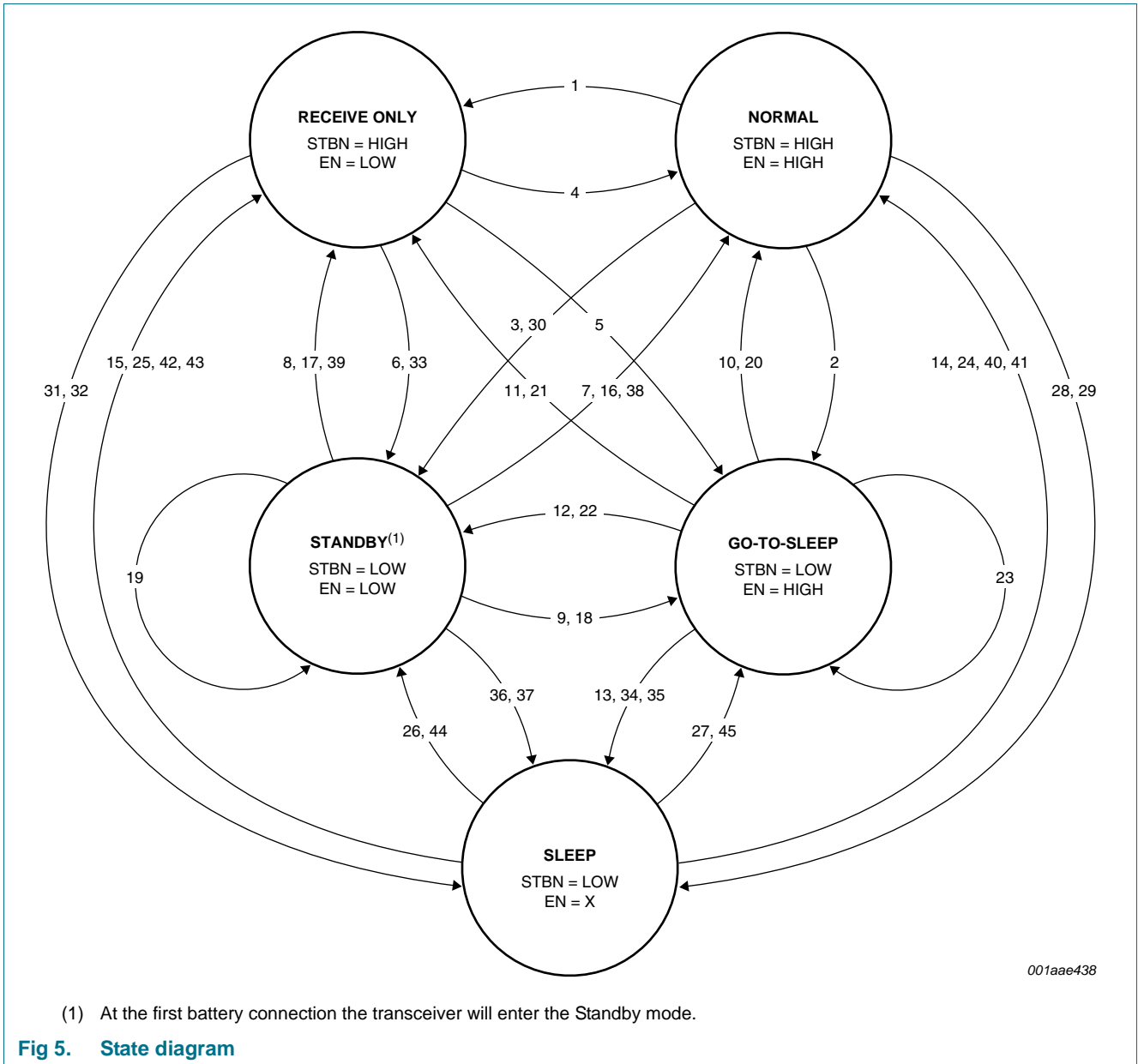


Fig 4. Timing diagram of control pins EN and STBN

The state diagram is shown in [Figure 5](#).



The state transitions are represented with numbers, which correspond with the numbers in column 3 of [Table 4](#) to [Table 7](#).

Table 4. State transitions forced by EN and STBN

→ indicates the action that initiates a transaction; 1→ and 2→ indicated the consequences of a transaction.

| Transition from mode | Direction to mode | Transition number | Pin | | Flag | | | | | Note |
|----------------------|-------------------|-------------------|------|-----|-------------------|--------------------|-------------------|---------|-------------|--------|
| | | | STBN | EN | UV _{VIO} | UV _{VBAT} | UV _{VCC} | PWON | Wake | |
| Normal | Receive-only | 1 | H | → L | cleared | cleared | cleared | cleared | cleared | |
| | Go-to-sleep | 2 | → L | H | cleared | cleared | cleared | cleared | cleared | |
| | Standby | 3 | → L | → L | cleared | cleared | cleared | cleared | cleared | [1] |
| Receive-only | Normal | 4 | H | → H | cleared | cleared | cleared | X | X | |
| | Go-to-sleep | 5 | → L | → H | cleared | cleared | cleared | X | X | |
| | Standby | 6 | → L | L | cleared | cleared | cleared | X | X | |
| Standby | Normal | 7 | → H | → H | cleared | cleared | 2 → cleared | X | 1 → cleared | [2][3] |
| | Receive-only | 8 | → H | L | cleared | cleared | 2 → cleared | X | 1 → set | [2][3] |
| | Go-to-sleep | 9 | L | → H | cleared | cleared | X | X | X | |
| Go-to-sleep | Normal | 10 | → H | H | cleared | cleared | cleared | X | 1 → cleared | [2][4] |
| | Receive-only | 11 | → H | → L | cleared | cleared | cleared | X | 1 → set | [2][4] |
| | Standby | 12 | L | → L | cleared | cleared | X | X | X | [4] |
| | Sleep | 13 | L | H | cleared | cleared | X | X | cleared | [5] |
| Sleep | Normal | 14 | → H | H | 2 → cleared | 2 → cleared | 2 → cleared | X | 1 → cleared | [2][3] |
| | Receive-only | 15 | → H | L | 2 → cleared | 2 → cleared | 2 → cleared | X | 1 → set | [2][3] |

[1] STBN must be set to LOW at least $t_{det(EN)}$ after the falling edge on EN.

[2] Positive edge on pin STBN sets the wake flag. In the case of a transition to Normal mode the wake flag is immediately cleared.

[3] Setting the wake flag clears the UV_{VIO}, UV_{VBAT} and UV_{VCC} flags.

[4] Hold time of go-to-sleep is less than $t_{h(gotosleep)}$.

[5] Hold time of go-to-sleep becomes greater than $t_{h(gotosleep)}$.

Table 5. State transitions forced by a wake-up

→ indicates the action that initiates a transaction; 1 → and 2 → indicated the consequences of a transaction.

| Transition from mode | Direction to mode | Transition number | Pin | | Flag | | | | | Note |
|----------------------|-------------------|-------------------|------|----|-------------------|--------------------|-------------------|------|-------|--------|
| | | | STBN | EN | UV _{VIO} | UV _{VBAT} | UV _{VCC} | PWON | Wake | |
| Standby | Normal | 16 | H | H | cleared | cleared | 1 → cleared | X | → set | [1] |
| | Receive-only | 17 | H | L | cleared | cleared | 1 → cleared | X | → set | [1] |
| | Go-to-sleep | 18 | L | H | cleared | cleared | 1 → cleared | X | → set | [1] |
| | Standby | 19 | L | L | cleared | cleared | 1 → cleared | X | → set | [1] |
| Go-to-sleep | Normal | 20 | H | H | cleared | cleared | 1 → cleared | X | → set | [1] |
| | Receive-only | 21 | H | L | cleared | cleared | 1 → cleared | X | → set | [1] |
| | Standby | 22 | L | L | cleared | cleared | 1 → cleared | X | → set | [1] |
| | Go-to-sleep | 23 | L | H | cleared | cleared | 1 → cleared | X | → set | [1] |
| Sleep | Normal | 24 | H | H | 1 → cleared | 1 → cleared | 1 → cleared | X | → set | [1][2] |
| | Receive-only | 25 | H | L | 1 → cleared | 1 → cleared | 1 → cleared | X | → set | [1][2] |
| | Standby | 26 | L | L | 1 → cleared | 1 → cleared | 1 → cleared | X | → set | [1] |
| | Go-to-sleep | 27 | L | H | 1 → cleared | 1 → cleared | 1 → cleared | X | → set | [1][2] |

[1] Setting the wake flag clears the UV_{VIO}, UV_{VBAT} and UV_{VCC} flags.

[2] Transition via Standby mode.

Table 6. State transitions forced by an undervoltage condition

→ indicates the action that initiates a transaction; 1→ and 2→ indicated the consequences of a transaction.

| Transition from mode | Direction to mode | Transition number | Flag | | | | | Note | |
|----------------------|-------------------|-------------------|-------------------|--------------------|-------------------|---------|---------|-------------|--------|
| | | | UV _{VIO} | UV _{VBAT} | UV _{VCC} | PWON | Wake | | |
| Normal | Sleep | 28 | → set | cleared | cleared | cleared | cleared | cleared | [1] |
| | Sleep | 29 | cleared | → set | cleared | cleared | cleared | cleared | [1] |
| | Standby | 30 | cleared | cleared | → set | cleared | cleared | cleared | [1] |
| Receive-only | Sleep | 31 | → set | cleared | cleared | X | X | 1 → cleared | [1] |
| | Sleep | 32 | cleared | → set | cleared | X | X | 1 → cleared | [1] |
| | Standby | 33 | cleared | cleared | → set | X | X | 1 → cleared | [1] |
| Go-to-sleep | Sleep | 34 | → set | cleared | cleared | X | X | 1 → cleared | [1] |
| | Sleep | 35 | cleared | → set | cleared | X | X | 1 → cleared | [1] |
| Standby | Sleep | 36 | → set | cleared | X | X | X | 1 → cleared | [1][2] |
| | Sleep | 37 | cleared | → set | X | X | X | 1 → cleared | [1][3] |

[1] UV_{VIO}, UV_{VBAT} or UV_{VCC} detected clears the wake flag.

[2] UV_{VIO} overrules UV_{VCC}.

[3] UV_{VBAT} overrules UV_{VCC}.

Table 7. State transitions forced by an undervoltage recovery
 → indicates the action that initiates a transaction; →1 and →2 are the consequences of a transaction.

| Transition from mode | Direction to mode | Transition number | Pin | | Flag | | | | | Note |
|----------------------|-------------------|-------------------|------|-----------|-------------------|--------------------|-------------------|---------|-------------|--------|
| | | | STBN | EN | UV _{VIO} | UV _{VBAT} | UV _{VCC} | PWON | Wake | |
| Standby | Normal | 38 | H | H | cleared | cleared | → cleared | X | X | [1] |
| | Receive-only | 39 | H | L | cleared | cleared | → cleared | X | X | [1] |
| Sleep | Normal | 40 | H | H | cleared | → cleared | cleared | X | 1 → cleared | [2][3] |
| | Normal | 41 | H | H | → cleared | cleared | cleared | X | X | [4] |
| | Receive-only | 42 | H | L | cleared | → cleared | cleared | X | 1 → set | [2][3] |
| | Receive-only | 43 | H | L | → cleared | cleared | cleared | X | X | [4] |
| | Standby | 44 | L | L | cleared | → cleared | cleared | X | 1 → set | [2][3] |
| | Sleep | 45 | L | X | → cleared | cleared | cleared | X | cleared | [4] |
| | Go-to-sleep | 46 | L | H | cleared | → cleared | cleared | X | 1 → set | [2][3] |
| Sleep | 47 | L | X | → cleared | cleared | cleared | X | cleared | [4] | |

[1] Recovery of UV_{VCC} flag.

[2] Recovery of UV_{VBAT} flag.

[3] Clearing the UV_{VBAT} flag sets the wake flag. In the case of a transition to Normal mode the wake flag is immediately cleared.

[4] Recovery of UV_{VIO} flag.

6.2.1 Normal mode

In Normal mode the transceiver is able to transmit and receive data via the bus lines BP and BM. The output of the normal receiver is directly connected to pin RXD.

Transmitter behavior in Normal mode, with no time-out present on pins TXEN and BGE and the temperature flag not set (TEMP HIGH = 0; see [Table 9](#)), is detailed in [Table 8](#).

In this mode, pin INH is set HIGH.

Table 8. Transmitter function table

| BGE | TXEN | TXD | Transmitter |
|-----|------|-----|---|
| L | X | X | transmitter is disabled |
| X | H | X | transmitter is disabled |
| H | L | H | transmitter is enabled; the bus lines are actively driven; BP is driven HIGH and BM is driven LOW |
| H | L | L | transmitter is enabled; the bus lines are actively driven; BP is driven LOW and BM is driven HIGH |

6.2.2 Receive-only mode

In Receive-only mode the transceiver can only receive data. The transmitter is disabled, regardless of the voltage levels on pins BGE and TXEN.

In this mode, pin INH is set HIGH.

6.2.3 Standby mode

Standby mode is a low-power mode featuring very low current consumption. In this mode, the transceiver cannot transmit or receive data. The low-power receiver is activated to monitor the bus for wake-up patterns.

A transition to Standby mode can be triggered by applying the appropriate levels on pins EN and STBN (see [Figure 5](#) and [Table 4](#)) or if an undervoltage is detected on pin V_{CC} (see [Figure 5](#) and [Section 6.2.5](#)).

In this mode, pin INH is set HIGH.

If the wake flag is set, pins RXEN and RXD are driven LOW; otherwise pins RXEN and RXD are set HIGH (see [Section 6.3](#)).

6.2.4 Go-to-sleep mode

In this mode, the transceiver behaves as in Standby mode. If this mode is selected for a time longer than the go-to-sleep hold time ($t_{h(\text{gotosleep})}$) and the wake flag has been previously cleared, the transceiver will enter Sleep mode, regardless of the voltage on pin EN.

6.2.5 Sleep mode

Sleep mode is a low-power mode. The only difference between Sleep mode and Standby mode is that pin INH is set floating in Sleep mode. A transition to Sleep mode will be triggered from all other modes if the UV_{VIO} flag or the UV_{VBAT} flag is set (see [Table 6](#)).

If an undervoltage is detected on pin V_{CC} or V_{BAT} while V_{IO} is present, the wake flag is set by a positive edge on pin STBN, provided that V_{IO} and (V_{CC} or V_{BAT}) are present.

The undervoltage flags will be reset when the wake flag is set, and the transceiver will enter the mode indicated by the levels on pins EN and STBN if V_{IO} is present.

6.3 Wake-up mechanism

From Sleep mode (pin INH is switched off), the transceiver will enter Standby or Go-to-sleep mode (depending on the level at pin EN) if the wake flag is set. Consequently, pin INH is switched on.

If an undervoltage is not detected on pins V_{IO} , V_{CC} and V_{BAT} , the transceiver will switch immediately to the mode indicated by the levels on pins EN and STBN.

In Standby, Go-to-sleep and Sleep modes, pins RXD and RXEN are driven LOW if the wake flag is set.

6.3.1 Remote wake-up

6.3.1.1 Bus wake-up via wake-up pattern

Bus wake-up is detected if two consecutive DATA_0 of at least $t_{det(wake)DATA_0}$ separated by an idle or DATA_1 of at least $t_{det(wake)idle}$, followed by an idle or DATA_1 of at least $t_{det(wake)idle}$ are present on the bus lines within $t_{det(wake)tot}$.

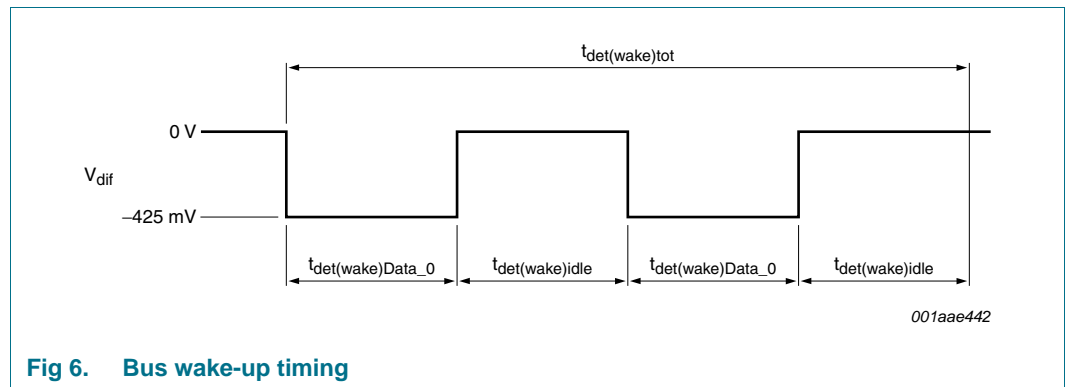


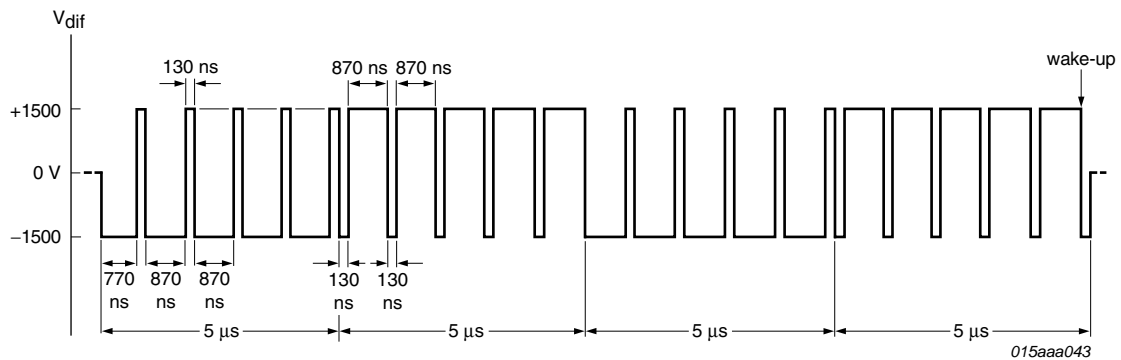
Fig 6. Bus wake-up timing

6.3.1.2 Bus wake-up via dedicated FlexRay data frame

The reception of a dedicated data frame, emulating a valid wake-up pattern, as shown in [Figure 7](#), sets the wake-up flag of the TJA1081.

Due to the Byte Start Sequence (BSS), preceding each byte, the DATA_0 and DATA_1 phases for the wake-up symbol are interrupted every 1 μ s. For 10 Mbit/s the maximum interruption time is 130 ns. Such interruptions do not prevent the transceiver from recognizing the wake-up pattern in the payload of a data frame.

The wake-up flag will not be set if an invalid wake-up pattern is received.



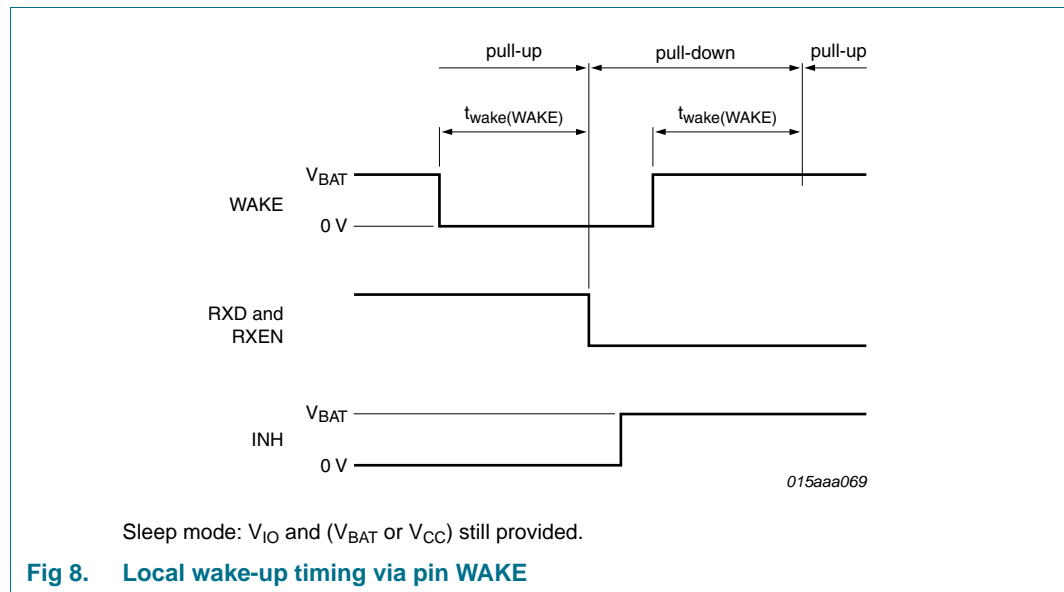
Each interruption is 130 ns.
 The transition time from DATA_0 to DATA_1 and from DATA_1 to DATA_0 is about 20 ns.
 The TJA1081 wake-up flag will be set with the following pattern:
 FFh, FFh, FFh, FFh, FFh, 00h, 00h, 00h, 00h, 00h,
 FFh, FFh, FFh, FFh, FFh, 00h, 00h, 00h, 00h, 00h,
 FFh, FFh, FFh, FFh, FFh, 00h, 00h, 00h, 00h, 00h,
 FFh, FFh, FFh, FFh, FFh, FFh

Fig 7. Minimum bus pattern for bus wake-up

6.3.2 Local wake-up via pin WAKE

If the voltage on pin WAKE is lower than $V_{th(det)(WAKE)}$ for longer than $t_{wake(WAKE)}$ (falling edge on pin WAKE) a local wake-up event on pin WAKE is detected. At the same time, the biasing of this pin is switched to pull-down.

If the voltage on pin WAKE is higher than $V_{th(det)(WAKE)}$ for longer than $t_{wake(WAKE)}$, the biasing of this pin is switched to pull-up, and no local wake-up will be detected.



Sleep mode: V_{IO} and (V_{BAT} or V_{CC}) still provided.

Fig 8. Local wake-up timing via pin WAKE

6.4 Fail-silent behavior

In order to be fail silent, undervoltage detection and a reset mechanism for the digital state machine are implemented.

If an undervoltage is detected on pins V_{CC} , V_{IO} and/or V_{BAT} , the transceiver will enter a low-power mode. This ensures the passive and defined behavior of the transmitter and receiver when an undervoltage is detected.

In the range between the minimum operating voltage and the undervoltage detection threshold, the principle functions of the transmitter and receiver are maintained. However, in this range parameters (e.g. thresholds and delays of the transmitter and receiver) may deviate from the levels specified for the operating range.

The digital state machine is supplied by V_{CC} , V_{IO} or V_{BAT} , depending on which voltage is available. Therefore, the digital state machine will be properly supplied as long as the voltage on pin V_{CC} or pin V_{IO} remains above 4.75 V or the voltage on pin V_{BAT} remains above 6.5 V.

If the voltage on all pins (i.e. V_{CC} , V_{IO} and V_{BAT}) breaks down, a reset signal will be given to the digital state machine as soon as the internal supply voltage for the digital state machine becomes too low for the proper operation of the state machine. This ensures the passive and defined behavior of the digital state machine in the event of an overall supply voltage breakdown.

6.4.1 V_{BAT} undervoltage

If the $UV_{V_{BAT}}$ flag is set, the transceiver will enter Sleep mode (pin INH is switched off) regardless of the voltages present on pins EN and STBN. If the undervoltage recovers, the wake flag will be set and the transceiver will enter the mode determined by the voltages on pins EN and STBN.

6.4.2 V_{CC} undervoltage

If the $UV_{V_{CC}}$ flag is set, the transceiver will enter Standby mode regardless of the voltages present on pins EN and STBN. If the undervoltage recovers or the wake flag is set, mode switching via pins EN and STBN is possible.

6.4.3 V_{IO} undervoltage

If the voltage on pin V_{IO} is lower than $V_{uvd(V_{IO})}$ (even if the $UV_{V_{IO}}$ flag is reset) pins EN, STBN, TXD and BGE are set LOW (internally) and pin TXEN is set HIGH (internally). If the $UV_{V_{IO}}$ flag is set, the transceiver will enter Sleep mode (pin INH is switched off). If the undervoltage recovers or the wake flag is set, mode switching via pins EN and STBN is possible.

6.5 Flags

6.5.1 Local wake-up source flag

The local wake-up source flag can only be set in a low-power mode. When a wake-up event is detected on pin WAKE (see [Section 6.3.2](#)), the local wake-up source flag is set. The local wake-up source flag is reset by entering a low-power mode.

6.5.2 Remote wake-up source flag

The remote wake-up source flag can only be set in a low-power mode if pin V_{BAT} is within its operating range. When a remote wake-up event is detected on the bus lines (see [Section 6.3.1](#)), the remote wake-up source flag is set. The remote wake-up source flag is reset by entering a low-power mode.

6.5.3 Wake flag

The wake flag is set if one of the following events occurs:

- The local or remote wake-up source flag is set (edge sensitive)
- A positive edge is detected on pin STBN when V_{IO} is present
- Recovery of the UV_{VBAT} flag

The wake flag is reset by entering Normal mode, a low-power mode or by setting one of the undervoltage flags.

6.5.4 Power-on flag

The PWON power-on flag is set if the internal supply voltage for the digital part becomes higher than the lowest value it needs to operate. Entering Normal mode resets the PWON flag.

6.5.5 Temperature medium flag

The temperature medium flag is set if the junction temperature exceeds $T_{j(warn)(medium)}$ in a normal-power mode while pin V_{BAT} is within its operating range. The temperature medium flag is reset when the junction temperature drops below $T_{j(warn)(medium)}$ in a normal-power mode with pin V_{BAT} within its operating range or after a read of the status register in a low-power mode while pin V_{BAT} is within its operating range. No action will be taken if this flag is set.

6.5.6 Temperature high flag

The temperature high flag is set if the junction temperature exceeds $T_{j(dis)(high)}$ in a normal-power mode while pin V_{BAT} is within its operating range.

The temperature high flag is reset if a negative edge is applied to pin TXEN while the junction temperature is lower than $T_{j(dis)(high)}$ in a normal-power mode with pin V_{BAT} within its operating range.

If the temperature high flag is set, the transmitter will be disabled.

6.5.7 TXEN_BGE clamped flag

The TXEN_BGE clamped flag is set if pin TXEN is LOW and pin BGE is HIGH for longer than $t_{detCL}(TXEN_BGE)$. The TXEN_BGE clamped flag is reset if pin TXEN is HIGH or pin BGE is LOW. If the TXEN_BGE flag is set, the transmitter is disabled.

6.5.8 Bus error flag

The bus error flag is set if pin TXEN is LOW and pin BGE is HIGH and the data received from the bus lines (pins BP and BM) are different to that received on pin TXD. The transmission of any valid communication element, including a wake-up pattern, does not lead to bus error indication.

The error flag is reset if the data on the bus lines (pins BP and BM) are the same as on pin TXD or if the transmitter is disabled. No action will be taken if the bus error flag is set.

6.5.9 UV_{V_{BAT}} flag

The UV_{V_{BAT}} flag is set if the voltage on pin V_{BAT} is lower than V_{uvd(V_{BAT})}. The UV_{V_{BAT}} flag is reset if the voltage is higher than V_{uvd(V_{BAT})} or by setting the wake flag; see [Section 6.4.1](#).

6.5.10 UV_{V_{CC}} flag

The UV_{V_{CC}} flag is set if the voltage on pin V_{CC} is lower than V_{uvd(V_{CC})} for longer than t_{det(uv)(V_{CC})}. The flag is reset if the voltage on pin V_{CC} is higher than V_{uvd(V_{CC})} for longer than t_{rec(uv)(V_{CC})} or the wake flag is set; see [Section 6.4.2](#).

6.5.11 UV_{V_{IO}} flag

The UV_{V_{IO}} flag is set if the voltage on pin V_{IO} is lower than V_{uvd(V_{IO})} for longer than t_{det(uv)(V_{IO})}. The flag is reset if the voltage on pin V_{IO} is higher than V_{uvd(V_{IO})} or the wake flag is set; see [Section 6.4.3](#).

6.5.12 Error flag

The error flag is set if one of the status bits S4 to S10 is set. The error flag is reset if none of the S4 to S10 status bits are set; see [Table 9](#).

6.6 Status register

The status register can be read out on pin ERRN by using pin EN as clock; the status bits are given in [Table 9](#). The timing diagram is shown in [Figure 9](#).

The status register is accessible if:

- UV_{V_{IO}} flag is not set and the voltage on pin V_{IO} is between 4.75 V and 5.25 V
- UV_{V_{CC}} flag is not set and the voltage on pin V_{IO} is between 2.2 V and 4.75 V

After reading the status register, if no edge is detected on pin EN for longer than t_{det(EN)}, the status bits (S4 to S12) will be cleared if the corresponding flag has been reset. Pin ERRN is LOW if the corresponding status bit is set.

Table 9. Status bits

| Bit number | Status bit | Description |
|------------|-------------------------------|---|
| S0 | LOCAL WAKEUP | local wake-up source flag is redirected to this bit |
| S1 | REMOTE WAKEUP | remote wake-up source flag is redirected to this bit |
| S2 | - | not used; always set |
| S3 | PWON | status bit set means PWON flag has been set previously |
| S4 | BUS ERROR | status bit set means bus error flag has been set previously |
| S5 | TEMP HIGH | status bit set means temperature high flag has been set previously |
| S6 | TEMP MEDIUM | status bit set means temperature medium flag has been set previously |
| S7 | TXEN_BGE CLAMPED | status bit set means TXEN_BGE clamped flag has been set previously |
| S8 | UV _{V_{BAT}} | status bit set means UV _{V_{BAT}} flag has been set previously |
| S9 | UV _{V_{CC}} | status bit set means UV _{V_{CC}} flag has been set previously |

Table 9. Status bits ...continued

| Bit number | Status bit | Description |
|------------|------------|---|
| S10 | UVVIO | status bit set means UV _{VIO} flag has been set previously |
| S11 | - | not used; always reset |
| S12 | - | not used; always reset |

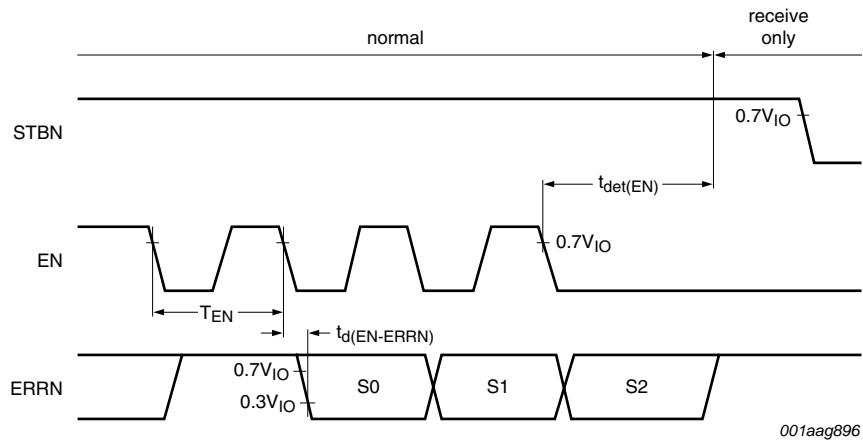


Fig 9. Timing diagram for status bits

7. Limiting values

Table 10. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are referenced to GND.

| Symbol | Parameter | Conditions | Min | Max | Unit | |
|----------------------|---------------------------------------|---------------------------------|------|------------------------|-------|----|
| V _{BAT} | battery supply voltage | no time limit | -0.3 | +60 | V | |
| | | operating range | 6.5 | 60 | V | |
| V _{CC} | supply voltage | no time limit | -0.3 | +5.5 | V | |
| | | operating range | 4.75 | 5.25 | V | |
| V _{IO} | supply voltage on pin V _{IO} | no time limit | -0.3 | +5.5 | V | |
| | | operating range | 2.2 | 5.25 | V | |
| V _{INH} | voltage on pin INH | | -0.3 | V _{BAT} + 0.3 | V | |
| I _{O(INH)} | output current on pin INH | no time limit | -1 | - | mA | |
| V _{WAKE} | voltage on pin WAKE | | -0.3 | V _{BAT} + 0.3 | V | |
| I _{O(WAKE)} | output current on pin WAKE | pin GND not connected | -15 | - | mA | |
| V _{BGE} | voltage on pin BGE | no time limit | -0.3 | +5.5 | V | |
| V _{TXEN} | voltage on pin TXEN | no time limit | -0.3 | +5.5 | V | |
| V _{TXD} | voltage on pin TXD | no time limit | -0.3 | +5.5 | V | |
| V _{ERRN} | voltage on pin ERRN | no time limit | -0.3 | V _{IO} + 0.3 | V | |
| V _{RXD} | voltage on pin RXD | no time limit | -0.3 | V _{IO} + 0.3 | V | |
| V _{RXEN} | voltage on pin RXEN | no time limit | -0.3 | V _{IO} + 0.3 | V | |
| V _{EN} | voltage on pin EN | no time limit | -0.3 | +5.5 | V | |
| V _{STBN} | voltage on pin STBN | no time limit | -0.3 | +5.5 | V | |
| V _{BP} | voltage on pin BP | no time limit | -60 | +60 | V | |
| V _{BM} | voltage on pin BM | no time limit | -60 | +60 | V | |
| V _{trt} | transient voltage | on pins BM and BP | [1] | -100 | - | V |
| | | | [2] | - | 75 | V |
| | | | [3] | -150 | - | V |
| | | | [4] | - | 100 | V |
| T _{stg} | storage temperature | | -55 | +150 | °C | |
| T _{vj} | virtual junction temperature | | [5] | -40 | +150 | °C |
| V _{ESD} | electrostatic discharge voltage | HBM on pins BP and BM to ground | [6] | -8.0 | +8.0 | kV |
| | | HBM at any other pin | [6] | -4.0 | +4.0 | kV |
| | | MM on all pins | [7] | -200 | +200 | V |
| | | CDM on all pins | [8] | -1000 | +1000 | V |

[1] According to ISO7637, test pulse 1, class C; verified by an external test house.

[2] According to ISO7637, test pulse 2a, class C; verified by an external test house.

[3] According to ISO7637, test pulse 3a, class C; verified by an external test house.

[4] According to ISO7637, test pulse 3b, class C; verified by an external test house.

[5] In accordance with IEC 60747-1. An alternative definition of T_{vj} is: $T_{vj} = T_{amb} + P \times R_{th(j-a)}$, where R_{th(j-a)} is a fixed value to be used for the calculation of T_{vj}. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).

[6] HBM: C = 100 pF; R = 1.5 kΩ.

[7] MM: C = 200 pF; L = 0.75 μH; R = 10 Ω.

[8] CDM: R = 1 Ω.

8. Thermal characteristics

Table 11. Thermal characteristics

| Symbol | Parameter | Conditions | Typ | Unit |
|---------------|---|-------------|-----|------|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | 118 | K/W |

9. Static characteristics

Table 12. Static characteristics

All parameters are guaranteed for $V_{BAT} = 6.5\text{ V to }60\text{ V}$; $V_{CC} = 4.75\text{ V to }5.25\text{ V}$; $V_{IO} = 2.2\text{ V to }5.25\text{ V}$; $T_{vj} = -40\text{ }^{\circ}\text{C to }+150\text{ }^{\circ}\text{C}$; $R_{bus} = 45\ \Omega$ unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------------------|---|--|-------------|-----|-------------|---------------|
| Pin V_{BAT} | | | | | | |
| I_{BAT} | battery supply current | low-power modes; no load on pin INH | - | - | 55 | μA |
| | | normal-power modes | - | - | 1 | mA |
| $V_{uvd(VBAT)}$ | undervoltage detection voltage on pin V_{BAT} | | 2.75 | - | 4.5 | V |
| Pin V_{CC} | | | | | | |
| I_{CC} | supply current | low-power modes | -1 | 0 | +10 | μA |
| | | Normal mode; $V_{BGE} = 0\text{ V}$; $V_{TXEN} = V_{IO}$; Receive-only mode | - | - | 15 | mA |
| | | Normal mode; $V_{BGE} = V_{IO}$; $V_{TXEN} = 0\text{ V}$ | - | - | 37 | mA |
| | | Normal mode; $V_{BGE} = V_{IO}$; $V_{TXEN} = 0\text{ V}$; $R_{bus} = \infty\ \Omega$ | - | - | 15 | mA |
| $V_{uvd(VCC)}$ | undervoltage detection voltage on pin V_{CC} | $(V_{BAT} \geq 5.5\text{ V AND } V_{IO} \geq 4.75\text{ V})$ OR $V_{BAT} \geq 6.5\text{ V}$ | 2.75 | 3.7 | 4.5 | V |
| Pin V_{IO} | | | | | | |
| I_{IO} | supply current on pin V_{IO} | low-power modes | -1 | +1 | +10 | μA |
| | | Normal and Receive-only modes; $V_{TXD} = V_{IO}$ | - | - | 1000 | μA |
| $V_{uvd(VIO)}$ | undervoltage detection voltage on pin V_{IO} | | 1 | 1.5 | 2 | V |
| $V_{uvr(VIO)}$ | undervoltage recovery voltage on pin V_{IO} | | 1 | 1.6 | 2.2 | V |
| $V_{uvhys(VIO)}$ | undervoltage hysteresis voltage on pin V_{IO} | $V_{BAT} > 5.5\text{ V}$ | 25 | - | 200 | mV |
| Pin EN | | | | | | |
| $V_{IH(EN)}$ | HIGH-level input voltage on pin EN | | $0.7V_{IO}$ | - | 5.5 | V |
| $V_{IL(EN)}$ | LOW-level input voltage on pin EN | | -0.3 | - | $0.3V_{IO}$ | V |
| $I_{IH(EN)}$ | HIGH-level input current on pin EN | $V_{EN} = 0.7V_{IO}$ | 3 | - | 11 | μA |
| $I_{IL(EN)}$ | LOW-level input current on pin EN | $V_{EN} = 0\text{ V}$ | -1 | 0 | +1 | μA |
| Pin STBN | | | | | | |
| $V_{IH(STBN)}$ | HIGH-level input voltage on pin STBN | | $0.7V_{IO}$ | - | 5.5 | V |

Table 12. Static characteristics ...continued

All parameters are guaranteed for $V_{BAT} = 6.5\text{ V to }60\text{ V}$; $V_{CC} = 4.75\text{ V to }5.25\text{ V}$; $V_{IO} = 2.2\text{ V to }5.25\text{ V}$; $T_{vj} = -40\text{ }^{\circ}\text{C to }+150\text{ }^{\circ}\text{C}$; $R_{bus} = 45\text{ }\Omega$ unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|---------------------------------------|---|-------------|------|----------------|---------------|
| $V_{IL(STBN)}$ | LOW-level input voltage on pin STBN | | -0.3 | - | $0.3V_{IO}$ | V |
| $I_{IH(STBN)}$ | HIGH-level input current on pin STBN | $V_{STBN} = 0.7V_{IO}$ | 3 | - | 11 | μA |
| $I_{IL(STBN)}$ | LOW-level input current on pin STBN | $V_{STBN} = 0\text{ V}$ | -1 | 0 | +1 | μA |
| Pin TXEN | | | | | | |
| $V_{IH(TXEN)}$ | HIGH-level input voltage on pin TXEN | | $0.7V_{IO}$ | - | 5.5 | V |
| $V_{IL(TXEN)}$ | LOW-level input voltage on pin TXEN | | -0.3 | - | $0.3V_{IO}$ | V |
| $I_{IH(TXEN)}$ | HIGH-level input current on pin TXEN | $V_{TXEN} = V_{IO}$ | -1 | 0 | +1 | μA |
| $I_{IL(TXEN)}$ | LOW-level input current on pin TXEN | $V_{TXEN} = 0.3V_{IO}$ | -15 | - | -3 | μA |
| $I_{L(TXEN)}$ | leakage current on pin TXEN | $V_{TXEN} = 5.25\text{ V}; V_{IO} = 0\text{ V}$ | -1 | 0 | +1 | μA |
| Pin BGE | | | | | | |
| $V_{IH(BGE)}$ | HIGH-level input voltage on pin BGE | | $0.7V_{IO}$ | - | 5.5 | V |
| $V_{IL(BGE)}$ | LOW-level input voltage on pin BGE | | -0.3 | - | $0.3V_{IO}$ | V |
| $I_{IH(BGE)}$ | HIGH-level input current on pin BGE | $V_{BGE} = 0.7V_{IO}$ | 3 | - | 11 | μA |
| $I_{IL(BGE)}$ | LOW-level input current on pin BGE | $V_{BGE} = 0\text{ V}$ | -1 | 0 | +1 | μA |
| Pin TXD | | | | | | |
| $V_{IH(TXD)}$ | HIGH-level input voltage on pin TXD | normal-power modes | $0.7V_{IO}$ | - | $V_{IO} + 0.3$ | V |
| $V_{IL(TXD)}$ | LOW-level input voltage on pin TXD | normal-power modes | -0.3 | - | $0.3V_{IO}$ | V |
| $I_{IH(TXD)}$ | HIGH-level input current on pin TXD | $V_{TXD} = V_{IO}$ | 70 | 230 | 650 | μA |
| $I_{IL(TXD)}$ | LOW-level input current on pin TXD | normal-power modes; $V_{TXD} = 0\text{ V}$ | -5 | 0 | +5 | μA |
| | | low-power modes | -1 | 0 | +1 | μA |
| $I_{LI(TXD)}$ | input leakage current on pin TXD | $V_{TXD} = 5.25\text{ V}; V_{IO} = 0\text{ V}$ | -1 | 0 | +1 | μA |
| $C_{i(TXD)}$ | input capacitance on pin TXD | not tested; with respect to [1] all other pins at ground; $V_{TXD} = 100\text{ mV}; f = 5\text{ MHz}$ | - | 5 | 10 | pF |
| Pin RXD | | | | | | |
| $I_{OH(RXD)}$ | HIGH-level output current on pin RXD | $V_{RXD} = V_{IO} - 0.4\text{ V};$ $V_{IO} = V_{CC}$ | -20 | - | -2 | mA |
| $I_{OL(RXD)}$ | LOW-level output current on pin RXD | $V_{RXD} = 0.4\text{ V}$ | 2 | - | 20 | mA |
| Pin ERRN | | | | | | |
| $I_{OH(ERRN)}$ | HIGH-level output current on pin ERRN | $V_{ERRN} = V_{IO} - 0.4\text{ V};$ $V_{IO} = V_{CC}$ | -1500 | -600 | -100 | μA |
| $I_{OL(ERRN)}$ | LOW-level output current on pin ERRN | $V_{ERRN} = 0.4\text{ V}$ | 300 | 700 | 1500 | μA |
| Pin RXEN | | | | | | |
| $I_{OH(RXEN)}$ | HIGH-level output current on pin RXEN | $V_{RXEN} = V_{IO} - 0.4\text{ V};$ $V_{IO} = V_{CC}$ | -4 | -1.7 | -0.5 | mA |
| $I_{OL(RXEN)}$ | LOW-level output current on pin RXEN | $V_{RXEN} = 0.4\text{ V}$ | 1 | 3.2 | 8 | mA |

Table 12. Static characteristics ...continued

All parameters are guaranteed for $V_{BAT} = 6.5\text{ V to }60\text{ V}$; $V_{CC} = 4.75\text{ V to }5.25\text{ V}$; $V_{IO} = 2.2\text{ V to }5.25\text{ V}$; $T_{vj} = -40\text{ °C to }+150\text{ °C}$; $R_{bus} = 45\ \Omega$ unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------------|--|--|--------------------|--------------------|--------------------|---------------|
| Pins BP and BM | | | | | | |
| $V_{o(idle)(BP)}$ | idle output voltage on pin BP | Normal or Receive-only mode; $V_{TXEN} = V_{IO}$ | 0.4V _{CC} | 0.5V _{CC} | 0.6V _{CC} | V |
| | | Standby, Go-to-sleep or Sleep mode | -0.1 | 0 | +0.1 | V |
| $V_{o(idle)(BM)}$ | idle output voltage on pin BM | Normal or Receive-only mode; $V_{TXEN} = V_{IO}$ | 0.4V _{CC} | 0.5V _{CC} | 0.6V _{CC} | V |
| | | Standby, Go-to-sleep or Sleep mode | -0.1 | 0 | +0.1 | V |
| $I_{o(idle)BP}$ | idle output current on pin BP | $-60\text{ V} \leq V_{BP} \leq +60\text{ V}$; with respect to GND and V_{BAT} | -7.5 | - | +7.5 | mA |
| $I_{o(idle)BM}$ | idle output current on pin BM | $-60\text{ V} \leq V_{BM} \leq +60\text{ V}$; with respect to GND and V_{BAT} | -7.5 | - | +7.5 | mA |
| $V_{o(idle)(dif)}$ | differential idle output voltage | | -25 | 0 | +25 | mV |
| $V_{OH(dif)}$ | differential HIGH-level output voltage | $40\ \Omega \leq R_{bus} \leq 55\ \Omega$; $V_{CC} = 5\text{ V}$; $C_{bus} = 100\text{ pF}$ | 600 | 850 | 1500 | mV |
| $V_{OL(dif)}$ | differential LOW-level output voltage | $40\ \Omega \leq R_{bus} \leq 55\ \Omega$; $V_{CC} = 5\text{ V}$; $C_{bus} = 100\text{ pF}$ | -1500 | -850 | -600 | mV |
| $V_{IH(dif)}$ | differential HIGH-level input voltage | normal-power modes; $-10\text{ V} \leq V_{BP} \leq +15\text{ V}$; $-10\text{ V} \leq V_{BM} \leq +15\text{ V}$ | 150 | 210 | 300 | mV |
| $V_{IL(dif)}$ | differential LOW-level input voltage | normal-power modes; $-10\text{ V} \leq V_{BP} \leq +15\text{ V}$; $-10\text{ V} \leq V_{BM} \leq +15\text{ V}$ | -300 | -210 | -150 | mV |
| | | low-power modes; $-10\text{ V} \leq V_{BP} \leq +15\text{ V}$; $-10\text{ V} \leq V_{BM} \leq +15\text{ V}$ | -400 | -210 | -125 | mV |
| $ \Delta V_{i(dif)(H-L)} $ | differential input volt. diff. betw. HIGH- and LOW-levels (abs. value) | normal-power modes; $(V_{BP} + V_{BM}) / 2 = 2.5\text{ V}$ | - | - | 10 | % |
| $ V_{i(dif)det(act)} $ | activity detection differential input voltage (absolute value) | normal-power modes | 150 | 210 | 300 | mV |
| $ I_{O(sc)} $ | short-circuit output current (absolute value) | on pin BP; $0\text{ V} \leq V_{BP} \leq 60\text{ V}$ | - | - | 35 | mA |
| | | on pin BM; $0\text{ V} \leq V_{BM} \leq 60\text{ V}$ | - | - | 35 | mA |
| | | on pins BP and BM; $V_{BP} = V_{BM}$; $0\text{ V} \leq V_{BP} \leq 60\text{ V}$; $0\text{ V} \leq V_{BM} \leq 60\text{ V}$ | - | - | 35 | mA |
| $R_{i(BP)}$ | input resistance on pin BP | idle level; $R_{bus} = \infty\ \Omega$ | 10 | 18.5 | 40 | k Ω |
| $R_{i(BM)}$ | input resistance on pin BM | idle level; $R_{bus} = \infty\ \Omega$ | 10 | 18.5 | 40 | k Ω |
| $R_{i(dif)(BP-BM)}$ | differential input resistance between pin BP and pin BM | idle level; $R_{bus} = \infty\ \Omega$ | 20 | 37 | 80 | k Ω |
| $I_{LI(BP)}$ | input leakage current on pin BP | $V_{BP} = 5\text{ V}$; $V_{BAT} = V_{CC} = V_{IO} = 0\text{ V}$ | -10 | 0 | +10 | μA |

Table 12. Static characteristics ...continued

All parameters are guaranteed for $V_{BAT} = 6.5\text{ V to }60\text{ V}$; $V_{CC} = 4.75\text{ V to }5.25\text{ V}$; $V_{IO} = 2.2\text{ V to }5.25\text{ V}$; $T_{vj} = -40\text{ °C to }+150\text{ °C}$; $R_{bus} = 45\ \Omega$ unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------------|--|--|-----------------|-----------------|-----------------|--------------------|
| $I_{L(BM)}$ | input leakage current on pin BM | $V_{BM} = 5\text{ V}$; $V_{BAT} = V_{CC} = V_{IO} = 0\text{ V}$ | -10 | 0 | +10 | μA |
| $V_{cm(bus)(DATA_0)}$ | DATA_0 bus common-mode voltage | $R_{bus} = 45\ \Omega$ | $0.4V_{CC}$ | $0.5V_{CC}$ | $0.6V_{CC}$ | V |
| $V_{cm(bus)(DATA_1)}$ | DATA_1 bus common-mode voltage | $R_{bus} = 45\ \Omega$ | $0.4V_{CC}$ | $0.5V_{CC}$ | $0.6V_{CC}$ | V |
| $\Delta V_{cm(bus)}$ | bus common-mode voltage difference | $R_{bus} = 45\ \Omega$ | -25 | 0 | +25 | mV |
| $C_{i(BP)}$ | input capacitance on pin BP | not tested; with respect to all other pins at ground; $V_{BP} = 100\text{ mV}$; $f = 5\text{ MHz}$ | [1] - | 8 | 15 | pF |
| $C_{i(BM)}$ | input capacitance on pin BM | not tested; with respect to all other pins at ground; $V_{BM} = 100\text{ mV}$; $f = 5\text{ MHz}$ | [1] - | 8 | 15 | pF |
| $C_{i(dif)(BP-BM)}$ | differential input capacitance between pin BP and pin BM | not tested; with respect to all other pins at ground; $V_{(BM-BP)} = 100\text{ mV}$; $f = 5\text{ MHz}$ | [1] - | 2 | 5 | pF |
| Pin INH | | | | | | |
| $V_{OH(INH)}$ | HIGH-level output voltage on pin INH | $I_{INH} = -0.2\text{ mA}$ | $V_{BAT} - 0.8$ | $V_{BAT} - 0.3$ | $V_{BAT} - 0.1$ | V |
| $I_{L(INH)}$ | leakage current on pin INH | Sleep mode | -5 | 0 | +5 | μA |
| $I_{OL(INH)}$ | LOW-level output current on pin INH | $V_{INH} = 0\text{ V}$ | -15 | -5 | -1 | mA |
| Pin WAKE | | | | | | |
| $V_{th(det)(WAKE)}$ | detection threshold voltage on pin WAKE | low-power mode | 2.5 | - | 4.5 | V |
| $I_{IL(WAKE)}$ | LOW-level input current on pin WAKE | $V_{WAKE} = 2.4\text{ V}$ for $t > t_{wake(WAKE)}$ | 3 | - | 11 | μA |
| $I_{IH(WAKE)}$ | HIGH-level input current on pin WAKE | $V_{WAKE} = 4.6\text{ V}$ for $t > t_{wake(WAKE)}$ | -11 | - | -3 | μA |
| Temperature protection | | | | | | |
| $T_{j(warn)(medium)}$ | medium warning junction temperature | $V_{BAT} > 5.5\text{ V}$ | 155 | 165 | 175 | $^{\circ}\text{C}$ |
| $T_{j(dis)(high)}$ | high disable junction temperature | $V_{BAT} > 5.5\text{ V}$ | 180 | 190 | 200 | $^{\circ}\text{C}$ |
| Power-on reset | | | | | | |
| $V_{th(det)POR}$ | power-on reset detection threshold voltage | | 3.0 | - | 3.4 | V |
| $V_{th(rec)POR}$ | power-on reset recovery threshold voltage | | 3.1 | - | 3.5 | V |
| $V_{hys(POR)}$ | power-on reset hysteresis voltage | | 100 | - | 200 | mV |

[1] These values are based on measurements taken on several samples (less than 10 pieces). These measurements have taken place in the laboratory and have been done at $T_{amb} = 25\text{ °C}$ and $T_{amb} = 125\text{ °C}$. No characterization has been done for these parameters. No industrial test will be performed on production products.

10. Dynamic characteristics

Table 13. Dynamic characteristics

All parameters are guaranteed for $V_{BAT} = 6.5\text{ V to }60\text{ V}$; $V_{CC} = 4.75\text{ V to }5.25\text{ V}$; $V_{IO} = 2.2\text{ V to }5.25\text{ V}$; $T_{vj} = -40\text{ }^{\circ}\text{C to }+150\text{ }^{\circ}\text{C}$; $R_{bus} = 45\ \Omega$ unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------------|--|--|-----|-----|-----|---------------|
| Pins BP and BM | | | | | | |
| $t_{d(TXD-bus)}$ | delay time from TXD to bus | Normal mode | [1] | | | |
| | | DATA_0 | - | - | 50 | ns |
| | | DATA_1 | - | - | 50 | ns |
| $\Delta t_{d(TXD-bus)}$ | delay time difference from TXD to bus | Normal mode; between DATA_0 and DATA_1 | [1] | - | 4 | ns |
| $t_{d(bus-RXD)}$ | delay time from bus to RXD | Normal mode; $C_{RXD} = 15\text{ pF}$; see Figure 11 | | | | |
| | | DATA_0 | - | - | 50 | ns |
| | | DATA_1 | - | - | 50 | ns |
| $\Delta t_{d(bus-RXD)}$ | delay time difference from bus to RXD | Normal mode $C_{RXD} = 15\text{ pF}$; between DATA_0 and DATA_1; see Figure 11 | - | - | 5 | ns |
| $t_{d(TXEN-busidle)}$ | delay time from TXEN to bus idle | Normal mode | - | 46 | 80 | ns |
| $t_{d(TXEN-busact)}$ | delay time from TXEN to bus active | Normal mode | - | 39 | 75 | ns |
| $t_{d(BGE-busidle)}$ | delay time from BGE to bus idle | Normal mode | - | 47 | 100 | ns |
| $t_{d(BGE-busact)}$ | delay time from BGE to bus active | Normal mode | - | 40 | 75 | ns |
| $t_{d(bus)(idle-act)}$ | bus delay time from idle to active | Normal mode | - | 7 | 30 | ns |
| $t_{d(bus)(act-idle)}$ | bus delay time from active to idle | Normal mode | - | 7 | 30 | ns |
| $t_{r(dif)(bus)}$ | bus differential rise time | 10 % to 90 %; $R_{bus} = 45\ \Omega$; $C_{bus} = 100\text{ pF}$ | 5 | 17 | 25 | ns |
| $t_{f(dif)(bus)}$ | bus differential fall time | 90 % to 10 %; $R_{bus} = 45\ \Omega$; $C_{bus} = 100\text{ pF}$ | 5 | 17 | 25 | ns |
| WAKE symbol detection | | | | | | |
| $t_{det(wake)DATA_0}$ | DATA_0 wake-up detection time | Standby or Sleep mode; | 1 | - | 4 | μs |
| $t_{det(wake)idle}$ | idle wake-up detection time | $-10\text{ V} \leq V_{BP} \leq +15\text{ V}$; $-10\text{ V} \leq V_{BM} \leq +15\text{ V}$ | 1 | - | 4 | μs |
| $t_{det(wake)tot}$ | total wake-up detection time | | 50 | - | 115 | μs |
| Undervoltage | | | | | | |
| $t_{det(uv)(VCC)}$ | undervoltage detection time on pin V_{CC} | | 100 | - | 670 | ms |
| $t_{rec(uv)(VCC)}$ | undervoltage recovery time on pin V_{CC} | | 1 | - | 5.2 | ms |
| $t_{det(uv)(VIO)}$ | undervoltage detection time on pin V_{IO} | | 100 | - | 670 | ms |
| $t_{det(uv)(VBAT)}$ | undervoltage detection time on pin V_{BAT} | | - | - | 1 | ms |
| Activity detection | | | | | | |
| $t_{det(act)(bus)}$ | activity detection time on bus pins | $V_{dif}: 0\text{ mV} \rightarrow 400\text{ mV}$ | 100 | - | 250 | ns |
| $t_{det(idle)(bus)}$ | idle detection time on bus pins | $V_{dif}: 400\text{ mV} \rightarrow 0\text{ mV}$ | 100 | - | 245 | ns |
| Mode control pins | | | | | | |
| $t_{d(STBN-RXD)}$ | STBN to RXD delay time | STBN HIGH to RXD HIGH; wake flag set | - | - | 2 | μs |

Table 13. Dynamic characteristics ...continued

All parameters are guaranteed for $V_{BAT} = 6.5\text{ V to }60\text{ V}$; $V_{CC} = 4.75\text{ V to }5.25\text{ V}$; $V_{IO} = 2.2\text{ V to }5.25\text{ V}$; $T_{vj} = -40\text{ °C to }+150\text{ °C}$; $R_{bus} = 45\ \Omega$ unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------|--------------------------------------|--|------|-----|-------|---------------|
| $t_{d(STBN-stb)}$ | delay time from STBN to standby mode | STBN LOW to Standby mode; Receive-only mode ^[2] | - | - | 10 | μs |
| $t_{h(gotosleep)}$ | go-to-sleep hold time | | 20 | 35 | 50 | μs |
| Status register | | | | | | |
| $t_{det(EN)}$ | detection time on pin EN | for mode control | 20 | - | 80 | μs |
| T_{EN} | time period on pin EN | for reading status bits | 4 | - | 20 | μs |
| $t_{d(EN-ERRN)}$ | delay time from EN to ERRN | for reading status bits | - | - | 2 | μs |
| WAKE | | | | | | |
| $t_{wake(WAKE)}$ | wake-up time on pin WAKE | low-power modes; falling edge on pin WAKE; $6.5\text{ V} \leq V_{BAT} \leq 27\text{ V}$ | 5 | 28 | 100 | μs |
| | | low-power modes; falling edge on pin WAKE; $27\text{ V} < V_{BAT} \leq 60\text{ V}$ | 25 | 75 | 175 | μs |
| Miscellaneous | | | | | | |
| $t_{detCL(TXEN_BGE)}$ | TXEN_BGE clamp detection time | | 2600 | - | 10400 | μs |

[1] Rise and fall time (10 % to 90 %) of $t_{r(TXD)}$ and $t_{f(TXD)} = 5\text{ ns} \pm 1\text{ ns}$.

[2] Same parameter is guaranteed by design for the transition from Normal to Go-to-sleep mode.

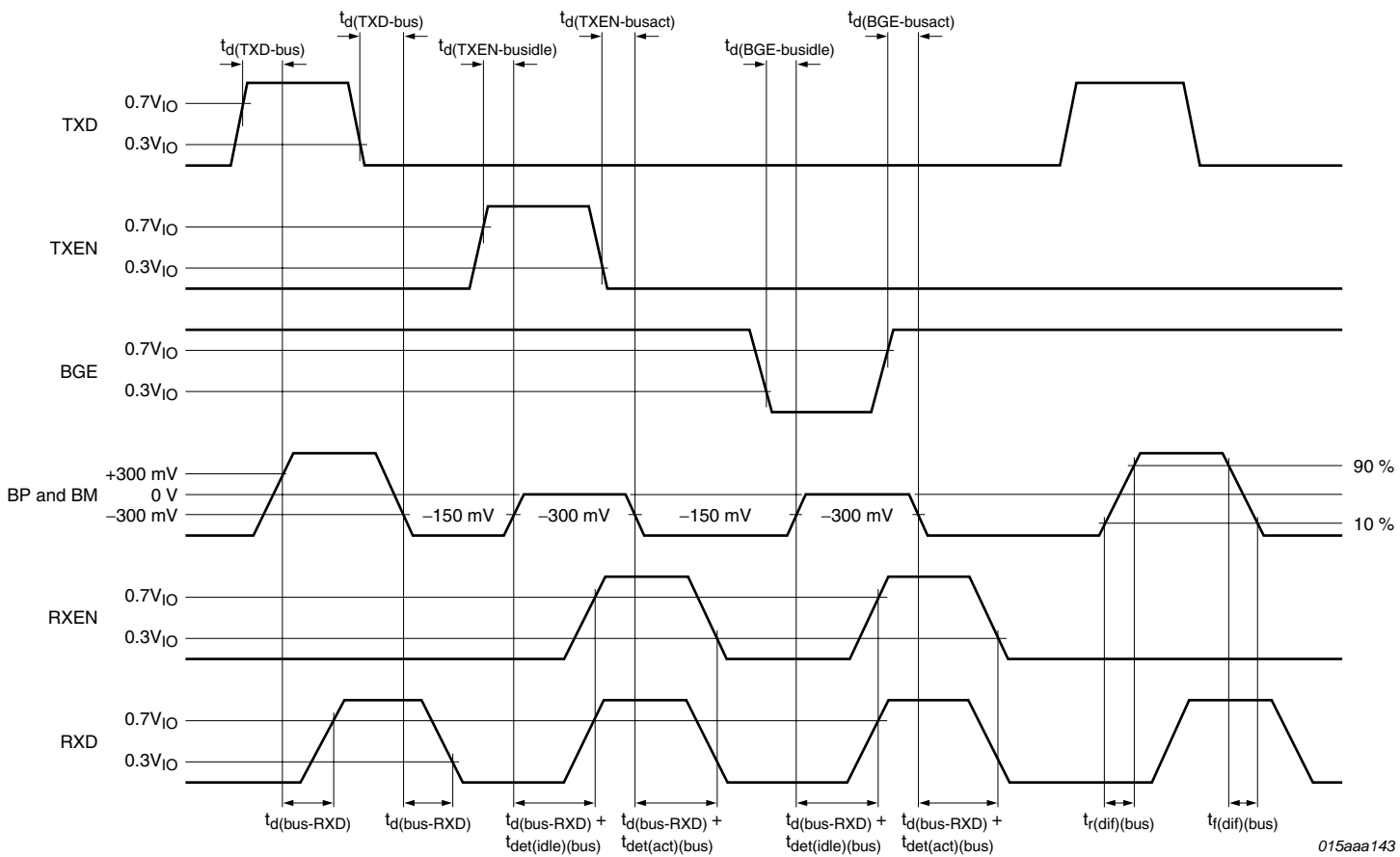
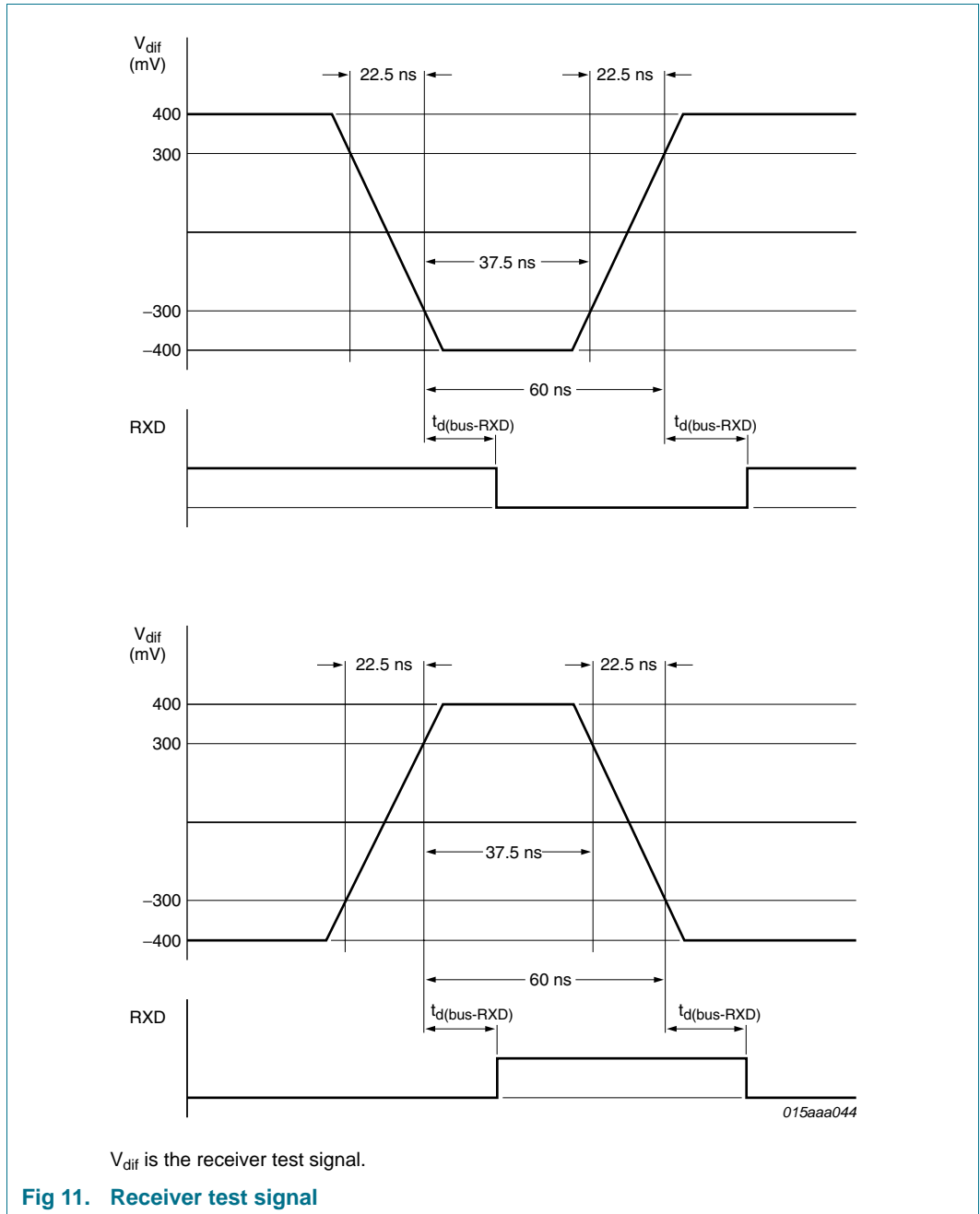


Fig 10. Detailed timing diagram



11. Test information

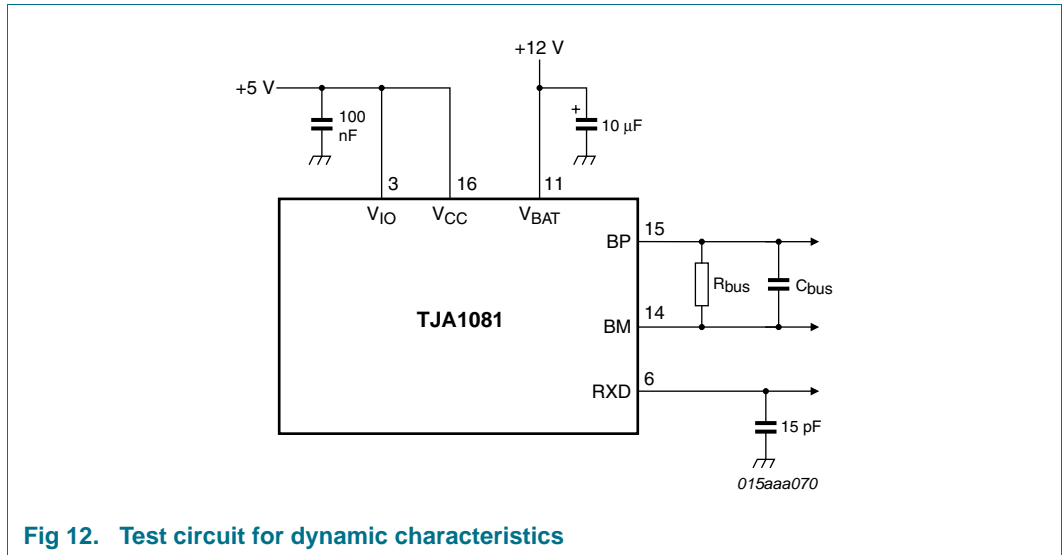


Fig 12. Test circuit for dynamic characteristics

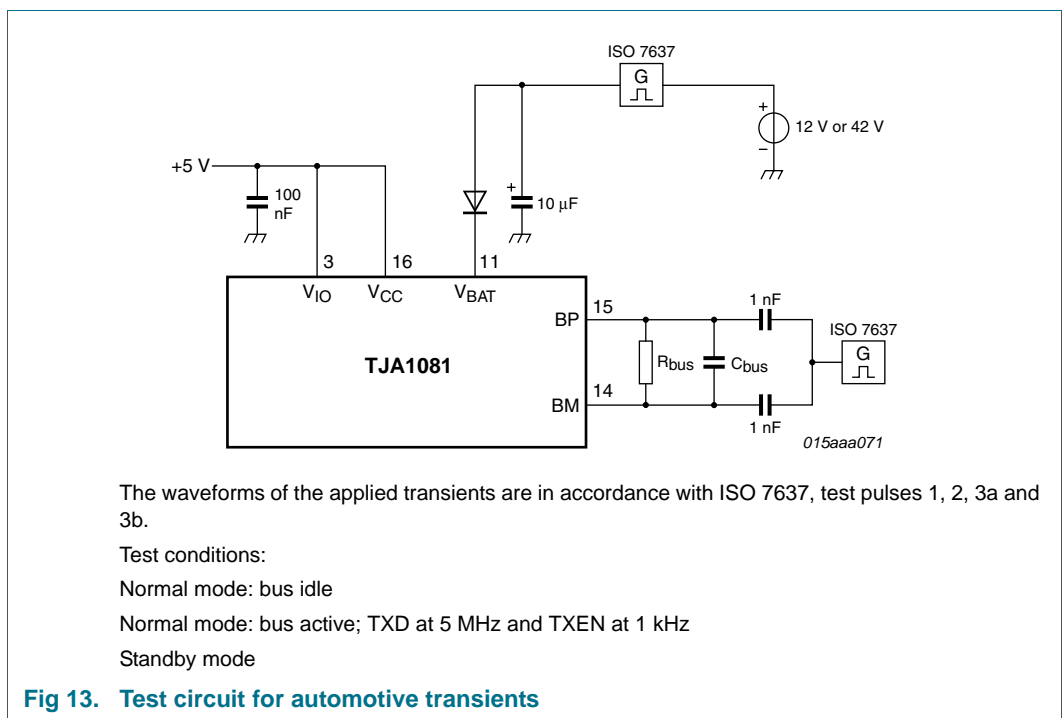


Fig 13. Test circuit for automotive transients

12. Package outline

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

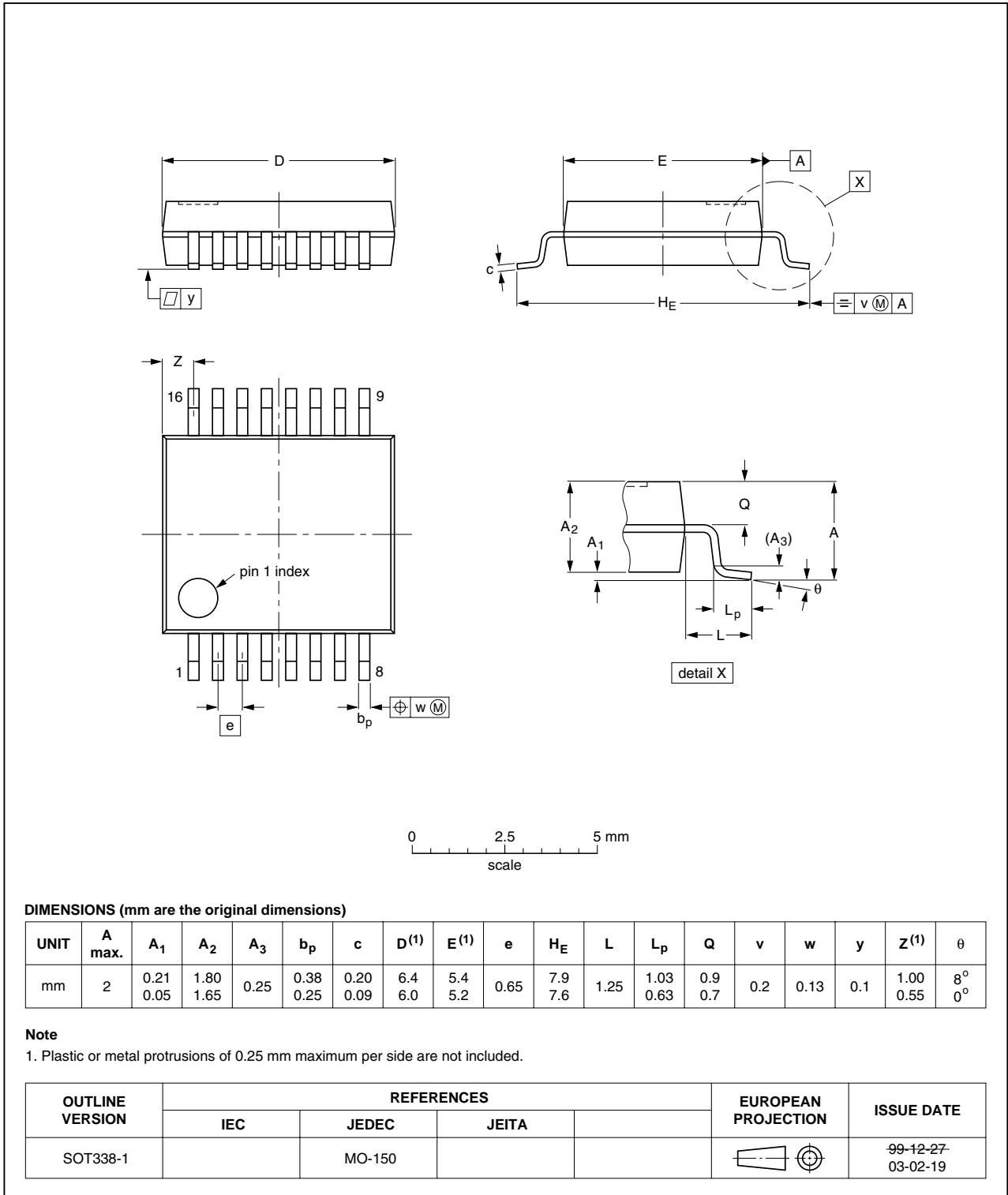


Fig 14. Package outline SOT338-1 (SSOP16)

13. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 15](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 14](#) and [15](#)

Table 14. SnPb eutectic process (from J-STD-020C)

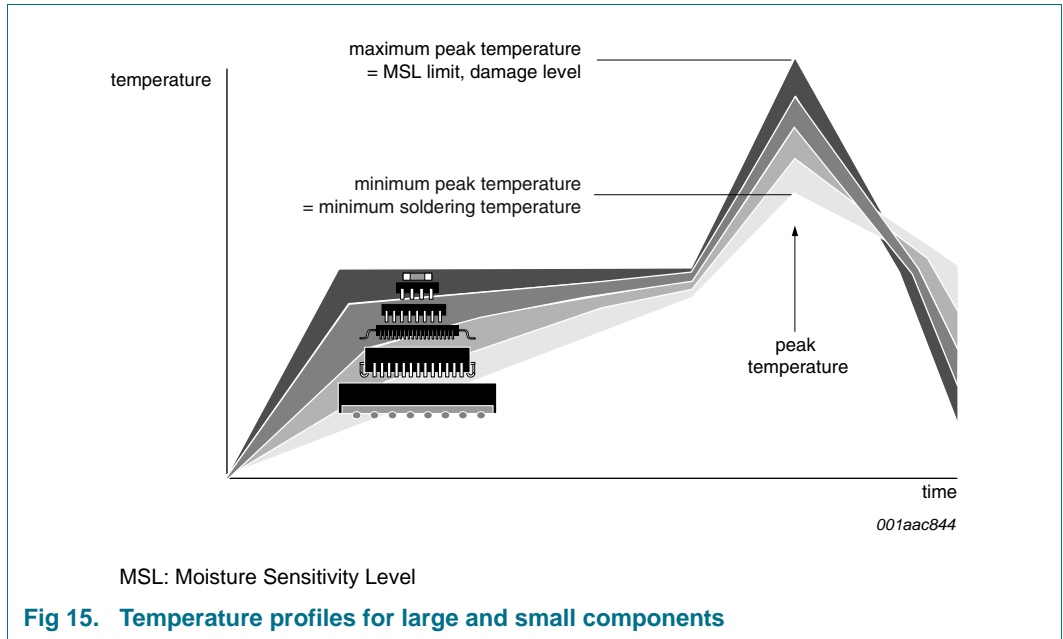
| Package thickness (mm) | Package reflow temperature (°C) | |
|------------------------|---------------------------------|-------|
| | Volume (mm ³) | |
| | < 350 | ≥ 350 |
| < 2.5 | 235 | 220 |
| ≥ 2.5 | 220 | 220 |

Table 15. Lead-free process (from J-STD-020C)

| Package thickness (mm) | Package reflow temperature (°C) | | |
|------------------------|---------------------------------|-------------|--------|
| | Volume (mm ³) | | |
| | < 350 | 350 to 2000 | > 2000 |
| < 1.6 | 260 | 260 | 260 |
| 1.6 to 2.5 | 260 | 250 | 245 |
| > 2.5 | 250 | 245 | 245 |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 15](#).



For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

14. Appendix

14.1 EPL 3.0.1 requirements implemented in the TJA1081

Table 16. EPL 3.0.1 requirements implemented

| EPL 3.0.1 parameter | Description |
|---|---|
| - | wake-up via dedicated data frames |
| R_{DCLoad} | transmitter output voltage defined for DC bus load of 40 Ω to 55 Ω /100 pF |
| dBDTx10, dBDTx01 | transmitter delay: ≤ 75 ns |
| uData0_LP | receiver thresholds for detecting DATA_0 in low-power modes: -400 mV (min)/ -100 mV (max) |
| dBDRxai | idle reaction time: 50 ns to 275 ns |
| dBDAActivityDetection | activity detection time 100 ns to 250 ns |
| dBDRxia | activity reaction time: 100 ns to 325 ns |
| uData1 - uData0 | receiver threshold mismatch: ≤ 30 mV |
| dBDRx10, dBDRx01 | receiver delay: ≤ 75 ns |
| dBusRx0BD, dBusRx1BD | minimum bit time: 70 ns |
| C_StarTxD, C_BDTxD | maximum input capacitance on pin TXD: 10 pF |
| dBDTxRxai | idle loop delay: ≤ 325 ns |
| - | BD_Off mode defined |
| | Short circuit currents: |
| iBP _{BMSHORTMax} , iBM _{BPSHORTMax} | BP shorted to BM: < 60 mA; no time limit |
| iBP _{GNDSHORTMax} , iBM _{GNDSHORTMax} | BP/BM shorted to ground: < 60 mA; no time limit |
| iBP _{-5SHORTMax} , iBM _{-5SHORTMax} | BP/BM shorted to -5 V: < 60 mA; no time limit |
| iBP _{BAT48SHORTMax} , iBM _{BAT27SHORTMax} | BP/BM shorted to 27 V: < 60 mA; no time limit |
| iBP _{BAT48SHORTMax} , iBM _{BAT27SHORTMax} | BP/BM shorted to 48 V: < 72 mA; no time limit |
| iBP _{BAT60SHORTMax} , iBM _{BAT60SHORTMax} | BP/BM shorted to 60 V: < 90 mA; for 400 ms (max) |
| dBDRV _{CC} | V _{CC} undervoltage recovery time: 10 ms (max) |
| uINH1 _{Not_Sleep} | voltage drop from V _{BAT} to INH: ≤ 1 V @ 200 μ A and V _{BAT} ≥ 5.5 V |
| iINH1 _{Leak} | leakage current, when INH is floating: ≤ 10 μ A |
| - | Qualification according to AEC-Q100 temperature classes |
| uESDExt | 6 kV ESD (min) on pins BP and BM according to HBM (100 pF/1500 Ω) |
| uESDInt | 2 kV ESD (min) on all other pins according to HBM (100 pF/1500 Ω) |

15. Abbreviations

Table 17. Abbreviations

| Abbreviation | Description |
|--------------|-------------------------------|
| BSS | Byte Start Sequence |
| CDM | Charged Device Model |
| ECU | Electronic Control Unit |
| EMC | ElectroMagnetic Compatibility |
| EME | ElectroMagnetic Emission |
| EMI | ElectroMagnetic Immunity |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TSS | Transmission Start Sequence |

16. References

- [1] **EPL** — FlexRay Communications System Electrical Physical Layer Specification Version 2.1 Rev. A, FlexRay Consortium, Dec. 2005
- [2] **EPL** — FlexRay Communications System Electrical Physical Layer Specification Version 3.0.1, FlexRay Consortium
- [3] **TJA1080A** — FlexRay transceiver data sheet, www.nxp.com

17. Revision history

Table 18. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|----------------|---|------------------------|---------------|-------------|
| TJA1081 v.4 | 20110224 | Product data sheet | - | TJA1081 v.3 |
| Modifications: | <ul style="list-style-type: none"> • Section 1, Section 2, Section 16: text revised • Table 10, Table 12, Table 13: parameter values/conditions/description/table notes revised • Figure 10: revised • Figure 13: figure note revised • Section 14 "Appendix": added • Ref. 2: added • Section 18 "Legal information": updated | | | |
| TJA1081 v.3 | 20090904 | Product data sheet | - | TJA1081 v.2 |
| TJA1081 v.2 | 20090728 | Product data sheet | - | TJA1081 v.1 |
| TJA1081 v.1 | 20090415 | Preliminary data sheet | - | - |

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| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
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| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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